IN THE CLAIMS:

Please amend the claims as follows:

1. (currently amended) An apparatus for outputting a clock signal for video reconstruction in a terminal, comprising:

an oscillator that generates the clock signal;

a control logic circuit with a phase locked loop for receiving an incoming video signal and phase locking to a clock signal portion of the incoming video signal, wherein the control logic circuit outputs a control signal for controlling an output of the oscillator based on the phase lock; and

A1 cont'd

a frequency range bounder in the phase locked loop that receives the control signal and outputs a bounded control signal that bounds the frequency of the oscillator to a selected range;

wherein the incoming video signal is a digital signal and the clock signal portion of the incoming video signal is program clock reference data for the digital signal.

2. (original) The apparatus of claim 1, wherein the frequency range bounder includes an output multiplexer and a threshold register that stores at least one threshold value and that is coupled to the output multiplexer, wherein the output multiplexer receives a control signal and outputs one of the control signal and said at least one threshold value as a bounded control signal to limit the frequency of the oscillator to the selected range.

3. (original) The apparatus of claim 2, wherein said at least one threshold register that stores at least one threshold value is a high limit register that stores an upper value and a low limit register that stores a lower value.

4. (original) The apparatus of claim 3, wherein the frequency range bounder includes an output multiplexer that selects one of the upper value, the control signal, and the lower value as the bounded control signal and outputs the bounded control signal to the oscillator to bound the oscillator frequency between an upper level and a lower level.

A1 cont'd

5. (original) The apparatus of claim 4, wherein the frequency range bounder includes at least one of a high comparator and a low comparator coupled to the output multiplexer, wherein the high comparator compares the control signal with a high limit and the low comparator compares the control signal with a low limit, and wherein the output multiplexer outputs the upper value as the bounded control signal if the control signal is above the high limit and outputs the lower value as the bounded control signal if the control signal is below the low limit.

6. (original) The apparatus of claim 3, wherein the frequency range bounder includes at least one of a minimum function block coupled to the high limit register and a maximum function block coupled to the low limit register, wherein the minimum function block outputs the smaller of the control signal and the upper value and wherein the maximum function block outputs the larger of the control signal and the lower value as the bounded control signal.

7. (original) The apparatus of claim 3, wherein the frequency range bounder includes a comparator coupled to the high limit register and low limit register, wherein the comparator compares the control signal with the upper and lower values and outputs the control signal to the output register if the control signal is between the upper and lower values.

A1 contd

8. (original) The apparatus of claim 7, wherein the frequency range bounder includes an output register coupled to the comparator, and wherein the comparator compares the control signal by comparing data values in the control signal with the upper and lower values and latching the data values in between the upper and lower values into the output register.

9. (original) The apparatus of claim 1, further comprising a drive circuit that receives the bounded control signal and that drives the oscillator in accordance with the bounded control signal.

10-19. (cancelled).

20. (currently amended) A method for outputting an oscillator-generated clock signal for video reconstruction in a terminal, comprising the steps of:

receiving an incoming video signal in a control logic circuit with a phase locked loop;

phase locking to a clock signal portion of the incoming video signal; and

limiting the oscillator frequency to a selected range using a frequency range bounder in the phase locked loop, wherein the frequency range bounder receives a control signal and limits the oscillator frequency based on the control signal;

wherein the incoming video signal is a digital signal and the clock signal portion of the incoming video signal is program clock reference data for the digital signal.

21. (original) The method according to claim 20, further comprising the step of outputting a bounded control signal from the frequency range bounder to the oscillator to conduct the limiting step.

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22. (original) The method of claim 20, wherein the limiting step has the step of selecting one of an upper value, the control signal, and a lower value as the bounded control signal.

23. (original) The method of claim 22, wherein the limiting step further has the steps of:

comparing the control signal with at least one of a high limit and a low limit;

outputting the upper value as the bounded control signal if the control signal is above the high limit; and

outputting the lower value as the bounded control signal if the control signal is below the low limit.

24-25. (cancelled)

26. (new) A circuit for controlling an oscillator that outputs a clock signal for video reconstruction, comprising:

a control logic circuit with a phase locked loop for receiving an incoming video signal and phase locking to a clock signal portion of the incoming video signal, wherein the control logic circuit outputs a control signal for controlling an output of the oscillator based on the phase lock; and

a frequency range bounder in the phase locked loop that receives the control signal and outputs a bounded control signal that bounds the frequency of the oscillator to a selected range;

A1 cont'd

wherein said frequency range bounder is configured to generate a high limit signal and a low limit signal and then select one of said control signal, said high limit signal or said low limit signal for transmission to said oscillator depending on whether said control signal remains within pre-defined high and low limits.

27. (new) The circuit of claim 26, further comprising a multiplexer which receives said control signal, said high limit signal and said low limit signal and selectively transmits said control signal, said high limit signal or said low limit signal to said oscillator depending on whether said control signal remains within pre-defined high and low limits.

28. (new) The circuit of claim 27, further comprising a high limit register for outputting said high limit signal and a low limit register for outputting said low limit signal.

29. (new) The circuit of claim 28, further comprising a high comparator for comparing said control signal and said high limit signal, wherein the output of said high comparator is provided to said multiplexer.

30. (new) The circuit of claim 28, further comprising a low comparator for comparing said control signal and said low limit signal, wherein the output of said low comparator is provided to said multiplexer.

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31. (new) The circuit of claim 26, further comprising:

a high limit register for outputting said high limit signal;

a low limit register for outputting said low limit signal; and

a comparator receiving said control signal, said high limit signal and said low limit signal;

wherein said comparator selects said control signal, said high limit signal or said low limit signal for transmission to said oscillator depending on whether said control signal remains within pre-defined high and low limits.

32. (new) The circuit of claim 26, further comprising:

a minimum function block configured to receive said control signal and said high limit signal, wherein said minimum function block selectively passes whichever signal is lower, said control signal or said high limit signal; and

a maximum function block configured to receive an output of said minimum function block and said low limit signal, wherein said maximum function block selectively passes

whichever signal is higher, said output from said minimum function block or said low limit signal, to said oscillator

33. (new) The circuit of claim 26, further comprising:

a maximum function block configured to receive said control signal and said low limit signal, wherein said maximum function block selectively passes whichever signal is higher, said control signal or said low limit signal; and

a minimum function block configured to receive an output of said maximum function block and said high limit signal, wherein said minimum function block selectively passes whichever signal is lower, said output from said maximum function block or said high limit signal, to said oscillator.

A' cont'd

34. (new) A method of controlling an oscillator that outputs a clock signal for video reconstruction, wherein said oscillator is controlled to remain within high and low frequency bounds, said method comprising:

receiving an incoming video signal and phase locking to a clock signal portion of the incoming video signal;

outputting a control signal for controlling an output of the oscillator based on the phase lock;

generating a high limit signal and a low limit signal; and

selecting one of said control signal, said high limit signal or said low limit signal for transmission to said oscillator depending on whether said control signal remains within pre-defined high and low limits.

35. (new) The method of claim 34, further comprising:

receiving said control signal, said high limit signal and said low limit signal with a multiplexer; and

with said multiplexer, selectively transmitting said control signal, said high limit signal or said low limit signal to said oscillator depending on whether said control signal remains within pre-defined high and low limits.

A1 cont'd

36. (new) The method of claim 35, further comprising:

comparing said control signal and said high limit signal with a high comparator; and

controlling said multiplexer with an output of said high comparator.

37. (new) The method of claim 35, further comprising:

comparing said control signal and said low limit signal with a low comparator; and

controlling said multiplexer with an output of said low comparator.

38. (new) The method of claim 34, further comprising:

receiving and comparing said control signal, said high limit signal and said low limit signal with a comparator; and

with said comparator, selecting said control signal, said high limit signal or said low limit signal for transmission to said oscillator depending on whether said control signal remains within pre-defined high and low limits.

39. (new) The method of claim 34, further comprising:

receiving said control signal and said high limit signal with a minimum function block;

with said minimum function block, selectively passing whichever signal is lower, said control signal or said high limit signal;

receiving an output of said minimum function block and said low limit signal with a maximum function block; and

with said maximum function block, selectively passing whichever signal is higher, said output from said minimum function block or said low limit signal, to said oscillator

A' cont'd

40. (new) The method of claim 34, further comprising:

receiving said control signal and said low limit signal with a maximum function block;

with said maximum function block, selectively passing whichever signal is higher, said control signal or said low limit signal;

receiving an output of said maximum function block and said high limit signal with a minimum function block; and

with said minimum function block, selectively passing whichever signal is lower, said output from said maximum function block or said high limit signal, to said oscillator

41. (new) A system for controlling an oscillator that outputs a clock signal for video reconstruction, wherein said oscillator is controlled to remain within high and low frequency bounds, said system comprising:

A1 cancel.

means for receiving an incoming video signal and phase locking to a clock signal portion of the incoming video signal;

means for outputting a control signal for controlling an output of the oscillator based on the phase lock;

means for generating a high limit signal and a low limit signal; and

means for selecting one of said control signal, said high limit signal or said low limit signal for transmission to said oscillator depending on whether said control signal remains within pre-defined high and low limits.